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| 10/750,843 | 01/05/2004 | Howard E. Rhodes | M4065.0947/P947 | 2490 |

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street, NW
Washington, DC 20037

| EXAMINER | |
|---|---|
| MONDT, JOHANNES P | |
| ART UNIT | PAPER NUMBER |
| 3663 | |

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/750,843 | RHODES, HOWARD E. | |
| | Examiner | Art Unit | |
| | Johannes P. Mondt | 3663 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *19-27 and 65-77* is/are pending in the application.

4a) Of the above claim(s) *73-77* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-27 and 65-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

Amendment filed 11/08/2005 forms the basis for this office action. In said Amendment Applicant cancelled claims 1-18 and 28-64, substantially amended claims 19-27 and added new claims 65-77. Comments on Remarks submitted with said Amendment are included under "Response to Arguments"; see below.

### *Election/Restrictions*

Newly submitted claims 73-77 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

The following inventions are restricted as patentably distinct inventions under 35 U.S.C. 121:

I. Claims 19-27 and 65-72, drawn to a method of operating a pixel cell, classified in class 348, subclass 311+.

II. Claims 73-77, drawn to a method of operating an imager, classified in class 257, subclass 290+.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because accumulation of charge at the

photo-conversion device as recited in claim19 is required in the combination (see claim 73). The subcombination has separate utility such as a single photodiode.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 73-77 have been withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. ***Claim 68*** recites the limitation "said pixel signal" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 19-27, 67 and 69-72*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al (6,326,230 B1) in view of Rhodes (6,140,630) (both made of record previously).

*On claim 19: Pain et al teach* a method for operating a pixel cell of an imager (title, abstract, col. 2, l. 64 – col. 3, l. 8 and claims 1-11 In Pain et al), the method comprising:

accumulating charge at a photo-conversion device 52 or 120 during an integration period (either photo-gate 52 of transistor PG: Figure 2A and col. 4, l. 39-43, or a photodiode 120: Figure 5A; and see claim 8 in Pain et al);

storing accumulated charge from said photo-conversion device at a charge collection region 54 via a transfer transistor TX (56) (Figures 2A and 5A; col. 4, l. 39-54 and col. 7, l. 15-16 and 56-63) (claim 8 in Pain et al: said charge collection region is the sense node);

reading out said charge from said charge collection region 45 (through transistors $M_{sel}$ and $M_{in}$ (col. 4, l. 58-66 and col. 7, l. 25-37); and

removing residual charge remaining in said photo-conversion device after said charge storage at said charge collection region (through signals to TX, TX2 (which is both transfer and reset transistor, "second transfer" transistor as recited because it is used to transfer charge, and reset transistor because it is used to help reset the charge remaining in said photo-conversion device) (col. 6, l. 33-40) (see claim 11 in Pain et al),

wherein said act of removing comprises activating a reset transistor (namely: reset transistors TX2) [N.B.: with regard to TX2 so-called second transfer transistor does structurally or functionally distinguish from a reset transistor, actually functioning to reset the charge in the photo-conversion device, hence said "second transfer" transistor 62 (N.B.: "gate" is merely *pars pro toto* for transistor) meets the

claim limitation "a reset transistor"] and said transfer transistor TX (56) prior to a subsequent integration period(column 3, lines 5-8).

*Pain et al do not necessarily teach* the limitation that said reading out is being conducted not merely to a sample circuit but to a sample and hold circuit. However, it would have been obvious to include said limitation in view of Rhodes who teaches said reading out to be conducted to a sample and hold circuit (S/H circuit within read circuit 60 in Figure 1: see col. 3, l. 57 – col. 4, l. 37) thus enabling comparisons of signals from different pixels by which pixels variations can be eliminated (col. 25-36).

*Motivation to* include the teaching by Rhodes is the ability to hold the signal after sampling with further processing steps such as signal subtraction to eliminate pixel variations.

. *On claim 20:* said act of removing comprises activating said reset transistor and said transfer transistor substantially simultaneously (see Fig. 6D, trace TX2 and trace TX for rest and transfer transistors, respectively).

*On claim 21:* said substantially simultaneous activation of said reset transistor TX2 and said transfer transistor TX occurs after said act of reading out said charge (Fig. 6D).

*On claim 22:* said act of transferring comprises transferring charge (through transistor TX2) from said photo-conversion device (either 52 or 120) to a supply voltage Vdd (col. 4, l. 49-54) and col. 7, l. 23-25).

*On claim 23:* the imager is a CMOS imager (col. 3, l. 38-55 and col. 4, l. 23-38).

*On claim 24:*the CMOS imager comprises a four-transistor, five-transistor, six transistor or seven transistor pixel architecture, as witnessed by transistors TX, TX2, RST already discussed, and source-follower transistor $M_{in}$ (col. 7, l. 25-37) and pixel selection switch transistor $M_{sel}$ (col. 7, l. 25-37).

*On claim 25:* said photo-conversion device 120 is a photodiode (col. 7, l. 5-21).

*On claim 26:* said photo-conversion device 52 is a photo-gate (col. 4, l. 39-47).

*On claim 27:* said photo-conversion device 52, being a photo-gate, inherently is a photoconductor, because conduction charges are produced by impinging but neutral light, whereby the conductivity of the photo-gate is changed.

*On claim 67:* reading out said charge from said charge collection region comprises operating a transistor ($M_{sel}$) for reading out said charge as a pixel signal to a read-out circuit 42 (column 4, lines 61-66 and Figure 1).

*On claims 69 and 72:* the method of Pain further comprises activating said rest transistor and said transfer transistor substantially simultaneously, comprising applying a rest signal to active a gate of said reset transistor TX2, and while said reset transistor is activated, applying a transfer signal to active a gate of said transfer transistor TX (see Fig. 6D) (hence claim 69 is met). Furthermore, the limitations provide jointly the full range of possible orderings of the activation times of reset and transfer signals that are physically possible except for one point infinitesimally close to said full range (namely: absolute simultaneity). Applicant evidently attaches patentable weight to the full range in two separate sub-ranges without explaining why said sub-ranges are preferable. Applicant's disclosure does not teach why the range, either of claim 69 or of claim 72, is

critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

*On claims 70-71:* In the method by Pain the transfer transistor is deactivated before said rest transistor (Fig. 6D). Furthermore, the limitations provide jointly the full range of possible orderings of the deactivation times of reset and transfer signals that are physically possible except for one point infinitesimally close to said full range (namely: absolute simultaneity). Applicant evidently attaches patentable weight to the full range in two separate sub-ranges without explaining why said sub-ranges are preferable. Applicant's disclosure does not teach why the range, either of claim 70 or of claim 71, is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

2. ***Claims 65-66 and 68*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al and Rhodes as applied to claim 19 above, and further in view of Ishida et al (6,046,466).

As detailed above, claim 19 is unpatentable over Pain et al in view of Rhodes. Neither necessarily teach the further limitations of claim 65 and 66. However, it would have been obvious to include said further limitations in view of Ishida et al, who in a patent on photoelectric conversion in a solid-state imaging device, hence analogous art,

teach the inclusion of resetting said charge collection region after the storage storage phase ("OPEN" phase of cycle, see Figure 24, for instance, and column 36, line 47 – column 37, line 46) through a single reset transistor (RST) in conjunction with a transfer transistor (TG) rather than two reset transistors.

*Motivation* to include the teaching by Ishida in this regard at least derives from the added economic advantage of using a single reset transistor and a single transfer transistor, thus reducing the complexity by at least one transistor (compare transistors TX, TX2 and RST in Pain et al). *Combination* of the teaching by Ishida et al easily is achieved by omitting and by assigning its function to the reset transistor in Pain et al. Said reset period is just prior to a subsequent integration period, as shown by Figure 24, and hence claim 66 is also met.

*On claim 68:* As detailed above, claim 66 is unpatentable over Pain et al in view of Rhodes. Pain et al do not necessarily teach the further limitation defined by claim 68. However, it would have been obvious to include said further limitation in view of Rhodes, who, in a patent incorporated by reference in Applicant's application of its relevance and hence analogous art, teach the inclusion of a load transistor 39 so as to provide an option to either load and collect the read charge through the sample and hold circuit or ground the sample. *Motivation* to include the teaching by Rhodes derives from the creation of said option.

### *Response to Arguments*

Applicant's arguments filed 11/08/2005 have been fully considered but they are not persuasive. First, new claims 73-77 are drawn to a different invention from the one elected by original representation, namely a combination of the elected sub-combination, and hence claims 73-77 are being withdrawn from consideration.

Second, both TX2 and RST are functionally reset transistors, as explained in the rejections above, with TX2 resetting the charge of the photo-conversion device and reset transistor SRT resetting the charge of the charge collection region.

Replacement Sheets for the Drawings and the amendment of the Specification have been approved. Accordingly, the objections to the Drawings and the Specification have been withdrawn.

The rejections in this office action have been provided at the earliest possible time.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
January 6, 2006

JACK KEITH
SUPERVISORY PATENT EXAMINER